In the Claims

Claims 1-13 (Canceled).

14 (Original). A process of forming a phase-change memory device comprising:

forming a recess in a substrate, wherein the recess exposes spaced-apart first and third active areas, and wherein the recess comprises a bottom and walls;

forming a polysilicon film in the recess; and

treating the polysilicon film to have a first conductivity at the bottom and a second conductivity at the walls.

15 (Original). The process according to claim 14, wherein treating comprises:

first angled doping the polysilicon film that is in contact with the first active area; and

second angled doping the polysilicon film that is in contact with the second active area.

16 (Original). The process according to claim 14, wherein treating further comprises doping the polysilicon film to form discrete isolated regions of the second conductivity.

17 (Original). The process according to claim 14, before treating, further comprising:

forming a temporary material in the recess; and

patterning the temporary material to expose the polysilicon film that is directly above the active areas.

18 (Original). The process according to claim 14, before treating, further comprising:

forming a temporary material in the recess;

patterning a mask over the temporary material; and

removing a portion of the temporary material to expose the polysilicon film that is directly above the active areas.

19 (Original). The process according to claim 14, further comprising:

forming a first isolation trench in the substrate to define spaced-apart first and second areas; and

forming a second isolation trench adjacent the first and second areas to define a third area.

20 (Original). The process according to claim 19, further comprising:

treating the first and third areas to form the first and third active areas.

21 (Original). The process according to claim 19, wherein the second isolation trench is orthogonal to the first isolation trench.

22 (Original). The process according to claim 19, wherein the second isolation trench is shallower than the first isolation trench.

23 (Original). The process according to claim 19, after forming the first isolation trench, further comprising:

filling the first isolation trench with an isolation dielectric; and

planarizing the substrate.

24 (Original). The process according to claim 19, after forming the first isolation trench, further comprising:

forming a thermal dielectric film in the first isolation trench;

filling the first isolation trench with an isolation dielectric; and

planarizing the substrate.

25 (Original). The process according to claim 19, after forming the second isolation trench, further comprising:

filling the second isolation trench with an isolation dielectric; and

planarizing the substrate.

26 (Original). The process according to claim 19, after forming the second trench, further comprising:

forming a thermal dielectric film in the second isolation trench;

filling the second isolation trench with an isolation dielectric; and

planarizing the substrate.

27 (Original). The process according to claim 19, further comprising:

forming a diode stack that is contiguous to the first isolation trench and the second isolation trench;

filling the first isolation trench and the second isolation trench; and

forming a self-aligned silicide layer upon the diode stack.

28 (Original). A process comprising:

forming a trench in a semiconductor substrate, wherein the trench exposes two active areas that are situated along the transverse axis of the trench, and wherein the trench exposes at least two active areas that are situated along the longitudinal axis of the trench; and

forming a phase-change memory element above each active area.

29 (Original). The process according to claim 28, further comprising:

forming a polysilicon film in the recess; and

treating the polysilicon film to have a first conductivity at the bottom and a second conductivity at the walls.

30 (Original). The process according to claim 28, wherein treating comprises:

first angled doping the polysilicon film that is in contact with the first active area; and

second angled doping the polysilicon film that is in contact with the second active area.

31 (Original). The process according to claim 28, wherein treating further comprises doping the polysilicon film to form discrete isolated regions of the second conductivity.

32 (Original). The process according to claim 28, before treating, further comprising:

forming a temporary material in the recess; and

patterning the temporary material to expose the polysilicon film that is directly above the active areas.

33 (Original). The process according to claim 28, before treating, further comprising:

forming a temporary material in the recess;

patterning a mask over the temporary material; and

removing a portion of the temporary material to expose the polysilicon film that is directly above the active areas.

34 (Original). The process according to claim 28, further comprising:

forming a polysilicon film in the recess; and

treating the polysilicon film to have a first conductivity at the bottom and a second conductivity at the walls;

planarizing the substrate to form electrode material;

modifying a portion of the electrode material so that the electrode material comprises a first portion having a first thermal coefficient of resistivity and a second portion having a different second thermal coefficient of resistivity.